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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,877	08/20/2001	Kiichi Yamashita	XA-9535	4057

7590 03/22/2004

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EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,877	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-16* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The amendment of Fig. 3A and abstract filed on February 04, 2004 have been received and entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 7, and 9-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaplan (US 4,321,648).

Regarding claim 1, Kaplan discloses a final stage of an overcurrent protection circuit for power transistors (see the solo Figure), wherein the circuit includes: a transistor (bipolar transistor T0) functions as an amplifying element; and a protection circuit (30) for detecting overcurrent of the base current of the transistor (T0) and if the detected base current of the transistor (T0) exceeds a predetermined set value from an idling current (that is the standby or initial base current of the transistor T0), and subtracting/withdrawing the overcurrent from nodes 22 & 24 via current mirrors circuits (T12-T14; and T16-T0) so that to prevent further increase in the base and collector currents of the transistor (T0) (see column 1, lines 49-68; and column 3, lines 10-25).

Regarding claims 2, 7, and 12, in addition to the teaching of the claim 1, Kaplan also discloses the overcurrent protection circuit of the final stage (see the rejection of claim 1) including a bias circuit (20) for providing a base current to the transistor (T0 – node 24) (see column 1, lines 49-68; and column 3, lines 20-26).

Regarding claim 3, Kaplan discloses a amplifier circuit (see the only Figure) comprising: a bipolar transistor (T0) for outputting an amplified signal; and a protection circuit (30) for detecting a base current of the transistor T0 increases from an idling current and exceeds a predetermined value and subtracting a detected amount of exceeding the predetermined value of the base current from the base current, and for controlling the base current such that the collector current of the transistor (T0) is restricted/limited to be equal or lower than a predetermined value (see column 3, lines 3-25).

Regarding claim 5, the bias/driver circuit of Kaplan includes a current source (transistor T10) coupled in series with a current mirror (T12 and T14).

Regarding claim 9, the circuit of Kaplan includes diodes (load 40) connected in parallel with the transistor T0 of a multiple stages (see the Figure).

Regarding claims 10-11, and 13-14, the amplifying element and protecting circuits of Kaplan comprises transistors (GaAs-HBT, Si-bipolar, and Si-MOSFET are also known transistors), which are integrated in to one single chip/component (see the Figure).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaplan (US 4,321,648) and the applicant admitted prior art (AAPA), Fig. 3A.

Regarding claim 4, Kaplan discloses the claimed invention of claim 2, including current mirror circuits, except for the matching circuit. The AAPA discloses (Fig. 3A) an amplifier circuit including matching circuits (4, 5). It would have been obvious to one person having ordinary skill in the art at the time the invention was made to include at least a matching circuit as suggested by the AAPA in the circuit of Kaplan for matching input/output signals.

Regarding claim 6, Kaplan discloses the claimed invention of the claim 2 except for the modification of the protection circuit, which includes resistors, transistors, and current mirrors. It would have been obvious to one person having ordinary skill in the art at the time the invention was made to modify such that to include resistors, transistors, and current mirrors as suggested by Kaplan, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

6. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama et al. (US 6,329,879) and Kaplan (US 4,321,648). Kaplan discloses the

claimed invention of claim 2. Maruyama et al. teaches/discloses (see Fig. 9) a wireless communication system including, inter alia, a high frequency amplifier (53), an antenna (57), a receiver (51), a frequency synthesizer (64), a voice-processing portion (62), a modulator (66), and a demodulator (68), wherein a voice signal (from the microphone 57), and amplified by a power amplifier and transmitted to an antenna (55). Therefore, it would have been obvious to one person having ordinary skill in the art at the time the invention was made to substitute the amplifier (53) as taught by Maruyama et al. with an overcurrent protection amplifier as taught by Kaplan for protecting the wireless communication system from being overloaded.

Allowable Subject Matter

7. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see the attached PTO-892).

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 703-605-4244. The examiner can normally be reached on 8:30 to 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN

Michael J. Tokar

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